UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/430,366	10/28/99	RAMSBEY M	M-7523-US

024251 MMC2/0815
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EXAMINER	
CHEN, J	
ART UNIT	**PAPER NUMBER**
2813	12

DATE MAILED: 08/15/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/430,366	Ramsbey et al.
Examiner	**Art Unit**
Jack Chen	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Aug 6, 2001*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 3-7, 9-12, and 14-20* is/are pending in the application.

4a) Of the above, claim(s) *16-20* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 3-7, 9-12, 14, and 15* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/6/2001 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 1, 5, 7, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitchell et al., U.S./4,713,142.

Mitchell et al. discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer

on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-5, cols. 1-6.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-7, 9-12, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956 or Yamagishi et al., U.S./5,808,339 or Chan et al., U.S./6,051,467 taken with Sze et al., "ULSI Technology" and in view of Applicant's admitted prior art.

Wu discloses a method for forming a semiconductor device having a substrate 200 and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer 204 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 on the substrate and the floating gate such that the

insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

Yamagishi et al. (figs. 9A-10D) discloses a method for forming a semiconductor device having a substrate 11 and a tunnel oxide 51 formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 53; depositing an insulator layer of oxide 54 on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 10A); and depositing a dielectric layer 55 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

Chan et al. discloses a method for forming a semiconductor device having a substrate 10 and a tunnel oxide 16 formed on the substrate, which comprises depositing a floating gate layer 18 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 18; depositing an insulator layer of oxide 30 on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 5); and depositing a dielectric layer on the planar surface directly (layer 32 is a optional

layer, which is well known in the art) over the exposed top surface of the floating gate and the insulator layer, see figs. 1-11, cols. 1-8.

However, the above references do not explicitly shows using high temperature oxide (Note: during the telephone interview dated on 8/3/2001, applicant admitted that this layer is well known in the art and it is formed by LPCVD process, also see the amendment dated on 8/6/2001, furthermore, applicant stated in the specification, other dielectric may used, i.e., see page 3, lines 26-30).

It is well known in the art to form the dielectric by using any CVD process. For example, Sze et al. teaches forming the dielectric by using LPCVD process, such will provide excellent purity and uniformity, confomal step coverage, large wafer capacity, high throughput, etc. Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

Furthermore, the thickness of claims 3 and 9 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width; the rate of etching, temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in energy, etching rate, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification.

> Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any thickness range suitable to the method in process of Wu or Yamagishi et al. or Chan et al. taken with Sze et al. and in view of Applicant's admitted prior art in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Wu or Yamagishi et al. or Chan et al. with the teaching of Sze et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device (also see above).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703)308-2417.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jack Chen

August 13, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800